AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1. (currently amended) A data recovery device comprising:

a number of sample components that obtain samples of data in a received encoded serial data stream at a number of phases, said received encoded serial data stream being a series of bits having a bit time period, indicating a data value by either a transition between two data levels or no transition during the bit time period, wherein the number of phases are successively offset throughout the ~~a~~ bit time period and the data samples are obtained throughout the bit time period at the number of phases;

a number of transition detectors ~~corresponding to the number of obtained samples~~ that analyze consecutive data samples in order to identify transitions by comparing pairs of successive data samples and generating a transition signal during a bit time period at a predetermined logic level when a successive pair of data samples have different data levels; and

a combining ~~first~~ circuit that generates a serial decoded data stream by combining the transition signals ~~that comprises values for time period(s) according to occurrence or non-occurrence of one or more transitions within the respective time period(s)~~.

2. (original) The device of claim 1, wherein the number of sample components are arranged in a dual column configuration to mitigate metastability.

3. (original) The device of claim 1, wherein the sample components are comprised of D-type flip flops respectively clocked at one of the number of phases.

4. (original) The device of claim 1, wherein the number of obtained samples is 12.

5. (original) The device of claim 1, wherein the transition detectors comprise an XOR logic that generates a low value on a non-occurrence of a transition between two associated successive samples and generates a high value on an occurrence of a transition between two associated successive samples and a register that maintains the generated value.

6. (original) The device of claim 1, wherein the transition detectors generate data toggles that indicate occurrence or non-occurrence of a transition for respective time periods.

7. (currently amended) The device of claim 6, wherein the combining ~~first~~ circuit performs a logical OR operation on the data toggles to generate the decoded data value.

8. (currently amended) The device of claim 7, wherein the combining ~~first~~ circuit substantially comprises one or more OR gates.

9. (original) The device of claim 1, further comprising a NRZI decoder that decodes the decoded data into non-encoded data.

10. (original) The device of claim 9, wherein the NRZI decoder decodes the decoded data with an inverter.

11. (original) The device of claim 1, further comprising an NRZI encoder that encodes the decoded data stream into an NRZI encoded data stream.

12. (currently amended) A clock and data recovery system comprising:

a receiver that receives an encoded a serial data stream having an associated frequency and said received serial data stream being a series of bits

having a bit time period, indicating a data value by either a transition between two data levels or no transition during the bit time period;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; ~~and~~

a sample component that obtains data samples of the received serial data stream at the N phases; and

a data recovery component that identifies transitions in the received serial data stream by comparing pairs of successive data samples and obtains a recovered serial data stream based solely on the identified transitions.

13. (original) The system of claim 12, further comprising a clock recovery component that recovers one or more clocks associated with the received serial data stream.

14. (original) The system of claim 13, wherein the clock recovery component is operable to identify a sample phase and a clock phase per bit of data.

15. (original) The system of claim 12, wherein the N phases are substantially evenly spaced.

16. (original) The system of claim 12, wherein N is equal to 8 and the time period is equal to about 2.08333 ns.

17. (currently amended) A method of recovering data from a received encoded serial data stream, said received encoded serial data stream being a series of bits having a bit time period, indicating a data value by either a transition between two data levels or no transition during the bit time period ~~over a single time period~~ comprising:

obtaining a number of data samples of the ~~a~~ received encoded serial data stream at each of ~~according to~~ a number of phase clocks, the phase clocks being

at the frequency of the received encoded serial data stream and successively offset throughout the bit time period;

analyzing consecutive data samples to identify transitions by comparing pairs of successive data samples;

generating a first value on identifying one or more transitions; and

generating a second value that is a complement of the first value on not identifying one or more transitions.

18-19. (canceled)

20. (original) The method of claim 17, wherein the first value is high and the second value is low.

21. (original) The method of claim 17, wherein analyzing consecutive samples comprises performing an exclusive-or operation on the consecutive samples.

22. (new) A data recovery device comprising:

a number of sample components that obtain samples of a received serial data stream at a number of phases, wherein the number of phases are successively offset throughout a bit time period and the samples are obtained throughout the time period at the number of phases;

a number of transition detectors corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions;

a first circuit that generates a serial decoded data stream that comprises values for time period(s) according to occurrence or non occurrence of one or more transitions within the respective time period(s); and

a NRZI decoder that decodes the decoded data into non-encoded data.

23. (new) The device of claim 22, wherein the NRZI decoder decodes the decoded data with an inverter.

24. (new) A data recovery device comprising:

a number of sample components that obtain samples of a received serial data stream at a number of phases, wherein the number of phases are successively offset throughout a bit time period and the samples are obtained throughout the time period at the number of phases;

a number of transition detectors corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions;

a first circuit that generates a serial decoded data stream that comprises values for time period(s) according to occurrence or non occurrence of one or more transitions within the respective time period(s); and

an NRZI encoder that encodes the decoded data stream into an NRZI encoded data stream.

25. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period;

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions; and

a clock recovery component that recovers one or more clocks associated with the received serial data stream, wherein the clock recovery component is operable to identify a sample phase and a clock phase per bit of data.

26. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; and

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions,

wherein the N phases are substantially evenly spaced.

27. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; and

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions,

wherein N is equal to 8 and the time period is equal to about 2.08333 ns.

28. (new) A method of recovering data over a single time period comprising:

obtaining a number of data samples of a received serial data stream according to a number of phase clocks;

analyzing consecutive data samples to identify transitions;

generating a first value on identifying one or more transitions; and

generating a second value that is a complement of the first value on not identifying one or more transitions,

wherein the phase clocks are successively offset so as to provide evenly spaces phases throughout a time period.

Claims 22-28 (Previous Claims 9-11, 14-16 and 19) in Mark-up Format

22. (new) A data recovery device comprising:

a number of sample components that obtain samples of a received serial data stream at a number of phases, wherein the number of phases are successively offset throughout a bit time period and the samples are obtained throughout the time period at the number of phases;

a number of transition detectors corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions;

a first circuit that generates a serial decoded data stream that comprises values for time period(s) according to occurrence or non occurrence of one or more transitions within the respective time period(s); and ~~The device of claim 1, further comprising~~

a NRZI decoder that decodes the decoded data into non-encoded data.

23. (new) The device of claim 22, wherein the NRZI decoder decodes the decoded data with an inverter.

24. (new) A data recovery device comprising:

a number of sample components that obtain samples of a received serial data stream at a number of phases, wherein the number of phases are successively offset throughout a bit time period and the samples are obtained throughout the time period at the number of phases;

a number of transition detectors corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions;

a first circuit that generates a serial decoded data stream that comprises values for time period(s) according to occurrence or non occurrence of one or more transitions within the respective time period(s); and ~~The device of claim 1, further comprising~~ an NRZI encoder that encodes the decoded data stream into an NRZI encoded data stream.

25. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period;

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions; and

a clock recovery component that recovers one or more clocks associated with the received serial data stream ~~The system of claim 13~~, wherein the clock recovery component is operable to identify a sample phase and a clock phase per bit of data.

26. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; and

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions ~~The system of claim 12~~,

wherein the N phases are substantially evenly spaced.

27. (new) A clock and data recovery system comprising:

a receiver that receives a serial data stream having an associated frequency;

a phase generator that produces N phases of a clock signal that have an associated frequency of about the frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; and

a data recovery component that identifies transitions in the received serial data stream and obtains a recovered serial data stream based solely on the identified transitions ~~The system of claim 12~~,

wherein N is equal to 8 and the time period is equal to about 2.08333 ns.

28. (new) A method of recovering data over a single time period comprising:

obtaining a number of data samples of a received serial data stream according to a number of phase clocks;

analyzing consecutive data samples to identify transitions;

generating a first value on identifying one or more transitions; and

generating a second value that is a complement of the first value on not identifying one or more transitions ~~The method of claim 17~~,

wherein the phase clocks are successively offset so as to provide evenly spaces phases throughout a time period.